



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/298,751	04/23/1999	SENG-KHOON TNG	ICEN-P001	2402
7590	11/05/2003		EXAMINER	
Susan Yee CARR & FERRELL 2225 EAST BAYSHORE ROAD SUITE 200 PALO ALTO, CA 94303			ODLAND, DAVID E	
			ART UNIT	PAPER NUMBER
			2662	
			DATE MAILED: 11/05/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)
	09/298,751	TNG ET AL.
	Examiner David Odland	Art Unit 2662

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 October 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) The period for reply expires 3 months from the mailing date of the final rejection.
- b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. The proposed amendment(s) will not be entered because:
 - (a) they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) they raise the issue of new matter (see Note below);
 - (c) they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: ____.

3. Applicant's reply has overcome the following rejection(s): _____.
4. Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. The a) affidavit, b) exhibit, or c) request for reconsideration has been considered but does NOT place the application in condition for allowance because: see continuation sheet.
6. The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. For purposes of Appeal, the proposed amendment(s) a) will not be entered or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

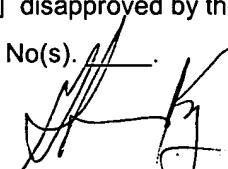
The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 1-14.

Claim(s) withdrawn from consideration: _____.

8. The proposed drawing correction filed on _____ is a) approved or b) disapproved by the Examiner.
9. Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). 
10. Other: _____.

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Art Unit: 2662

Continuation of 5: On page 2 paragraph 3, regarding the 35 U.S.C. 102(e) rejection of claims 1,7,9 and 11-14, the Applicant argues that Nguyen does not teach or suggest a second circuit directly connected to outputs from the first circuit because Nguyen shows intermediate AND gates and inverters. The Examiner respectfully disagrees. The claim does not recite that the circuit must only include a single electrical element. In this case, Nguyen discloses in figure 3A a circuit comprising, *inter alia*, AND gates 314,335 and 322, inverter 331, MUX 337 and OR gate 348, wherein the inputs to the circuit are lines 313,327, a logic '0', 315 and 314 and the output of the circuit is 352. This secondary circuit is directly connected to the output of both of the barrel shifters 301 and 302. Thus Nguyen does indeed teach of a secondary circuit directly connected to the first circuit.

Furthermore, on page 2 paragraph 3 through page 3 paragraph 1, the Applicant argues that the Examiner has incorrectly asserted that the AND gates and inverters can be considered part of the MUX and that they are selection logic for the MUX. Conversely, the Applicant asserts that this differs from the Nguyen disclosure because Nguyen uses control lines 345-348 to select the MUX inputs. It appears as though the Applicant has incorrectly interpreted the Examiners previous assertions. To clarify the Examiners previous assertions, the AND gates and the inverters are used to select the proper signals to be sent to the *inputs* of the MUX, after which the control signals are used to select the proper input that is to be *output* from the MUX. Thus the AND gates and inverters are used as selection logic, such that the proper input signals to the MUX are chosen. Furthermore, the AND gates and inverters can and are being considered as part of the same 'secondary circuit', as recited in the claim. Note the claim does not restrict the secondary circuit to include only a single element. In fact, dependent claim 3 recites that the

Art Unit: 2662

secondary circuit *comprises at least one multiplexer*. The term ‘comprises’ and ‘at least one’ imply that the second circuit includes other elements, such as additional multiplexers. Therefore, Nguyen does indeed disclose that the second circuit is connected to the first circuit.

On page 4 paragraph 2, regarding the 35 U.S.C. 103(a) rejection of claim 2, The Applicant argues that one skilled in the art would not have used the apparatus taught in Nguyen to receive a plurality of channels because the data shifting in Nguyen are of operands for instructions and thus having interleaved channels as the operands is illogical because they would have corrupt data for the logical operations. The Examiner respectfully disagrees. There is no teaching or suggestion in Nguyen to would lead one to conclude that the operands must only be of a single channel and cannot be modified to utilizing a plurality of interleaved channels. In fact, Nguyen seems to imply the opposite. In columns 1 lines 10-19, Nguyen discloses that the invention is implemented with respect to multimedia applications, which comprise data such as audio and video data streams and the invention also uses an SIMD architecture that comprises a single-instruction multiple-data configuration. Thus processing an interleaved plurality of channels would certainly be a logical modification in order to accommodate the multimedia, multiple-data formats of Nguyen. Furthermore, multimedia data requires a high Quality-Of-Service level in order to maintain the timing/delay constraints that are associated with such data. Therefore, receiving and processing a plurality of interleaved multimedia channels will allow Nguyen to operate faster and more efficiently rather than only receiving data from a single data stream. This would thus aid the system in maintaining the Quality-Of-Service requirements.

Lastly, on page 4 paragraph 3, regarding the 35 U.S.C. 103(a) rejection of claim 3, the Applicant contends that Nguyen is not a proper reference because it does not disclose that the

Art Unit: 2662

multiplexer is directly connected to the barrel shift register. The Examiner respectfully disagrees. The claim *does not* recite that multiplexer must be *directly* connected to the barrel shift register. The claim merely recites that the multiplexer is ***selectably connected*** (emphasis added) to the barrel shift register. Nguyen clearly shows that the output signal of shift register 302 is connected to the AND gate 322 which is used to *select* this signal in accordance with the masking signal received from the inverter 331 and this signal is then sent as an input to the multiplexer 337 (see figure 3A and column 4 lines 32-65). Therefore, the multiplexer is indeed ‘selectably connected’ to the barrel shifter.

Note, if the Applicant feels an interview would expedite the handling of this case, the Applicant is invited to contact the Examiner at 703-305-3231.